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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/668,472

09/22/2003

Walter Beck

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EXAMINER

TALBOT, BRIAN K

ART UNIT

PAPER NUMBER

1715

MAIL DATE

DELIVERY MODE

06/04/2010

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/668,472	Applicant(s) BECK ET AL.	
	Examiner Brian K. Talbot	Art Unit 1715	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 March 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,4-8 and 11-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,4-8 and 11-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>3/9/10</u> . | 6) <input type="checkbox"/> Other: _____ |

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1. The amendment filed 3/9/10 has been considered and entered. Claims 23 and 24 are newly added. Claims 2,3,9,10 and canceled. Claims 1,4-8 and 11-24 remain in the application.

2. The amendment filed 11/9/09 has been considered and entered. Claims 2,3,9,10 have been canceled. Claims 1,4-8 and 11-24 remain in the application.

Claim Rejections - 35 USC § 103

3. Claims 1,4-8 and 11-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (U.S. Patent 6,406,939, hereafter '939) (a) in view of Zuniga-Ortiz et al. (U.S. Patent Application Publication 2003/0080392, hereafter '392) and Bayan et al. (U.S. Patent 6,372,539, hereafter '539) or (b) in view of Applicant's admitted state of the art (pg. 1, lines 5-13) both (a) and (b) further in combination with Djokic et al. (5,849,170).

Claims 1 and 6: '939 teaches an example which teaches
a method for producing a conductive coating on a dielectric (i.e. insulating) substrate
(col. 3, lines 43-53), comprising:

equipping, in selected regions, at least one surface of an electrically insulating substrate
(401) with a coating of an electrically highly conductive first metal (402), the coating being
structured as a printed circuit board;

cleaning the at least one coated surface (col. 6, lines 42-46);

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seeding the coating with seeds of a second metal (Ni) and then depositing a layer including an alloy (Ni-P) of the second metal onto the coating seeded with the seeds of the second metal via electroless plating (col. 6, lines 50-55).

The electrolessly plated metal may include palladium alloys (col. 4, lines 6-11).

‘939 does not explicitly teach that this substrate is subjected to firing. However, the examiner takes Official Notice that it is well known in the art of printed circuit components to fire components to bond them to one another after formation of the components. See, e.g., ‘939 col. 8, lines 34-40.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have bonded the product of Example 2 to another substrate via a firing process because it is well known in the art to use such processes in order to join printed circuit components together.

(a) ‘939 is discussed above. It teaches that the substrate may be a ceramic (col. 4, line 63-col. 5, line 2), but does not teach that the first metal includes silver.

However, silver is a well known material for terminal bonding pads. See, e.g., ‘392, claim 23. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a terminal pad including silver as the particular terminal pad of ‘939 with a reasonable expectation of success because ‘392 teaches that silver is a suitable material for terminal pads. The selection of something based on its known suitability for its intended use has been held to support a *prima facie* case of obviousness. *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945).

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‘939 teaches that the product may be subjected to connection technologies such as wire bonding, but ‘939 and ‘392 do not explicitly teach contacting a gold bonding wire to the first metal.

However, ‘539 teaches that gold wires may be used as connection technologies for circuit components, and that gold forms a sufficient bond with silver (col. 4, lines 38-50). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a gold bonding wire as the particular connection technology of ‘939 for attaching at least one chip because ‘939 teaches that wire bonding is a conventional connection technology and because ‘539 teaches that gold wires in particular are suitable for successful bonding to silver.

(b) ‘939 fails to teach the metallization paste to be silver, gold or silver alloys.

Applicant’s admitted state of the art (pg. 1, lines 5-13) teaches that it is well known in the art that “in modern electronics, the trend is toward a greater and greater reduction in component sizes and toward the integration of passive components as well, so that existing requirements in terms of increasing integration density of integrated circuits can be met. One promising technology for achieving this goal is so-called low-temperature co-fired ceramic (LTCC), known for example from the periodical "productronic" 8, 1995, pp. 40 ff. LTCC refers to a glass-ceramic mixture that, together with metallization pastes made e.g. from Ag, AgPd, or Au, is fired at a relatively low temperature that is below the melting point of the aforesaid metals.

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Therefore it would have been obvious for one skilled in the art to have utilized silver, gold or a silver alloy as evidenced by Applicant's admitted state of the art (pg. 1, lines 5-13) with the expectation of increasing integration density of integrated circuits as detailed above.

Lin (U.S. Patent 6,406,939, hereafter '939) (a) in view of Zuniga-Ortiz et al. (U.S. Patent Application Publication 2003/0080392, hereafter '392) and Bayan et al. (U.S. Patent 6,372,539, hereafter '539) or (b) in view of Applicant's admitted state of the art (pg. 1, lines 5-13) fail to teach forming a second metal layer atop the first metal layer.

Djokic et al. (5,849,170) teaches electroless/electrolytic method for preparation of metallized ceramic substrates. Djokic et al. (5,849,170) teaches a ceramic substrate being cleaned, sensitized with palladium sites, electroless plating palladium and/or silver, electrolytically plating the same palladium and/or silver to increase thickness of the layer and finally electrodepositing a metal alloy including palladium and/or silver (col. 2, lines 30-55 and col. 5, lines 55-65).

Therefore it would have been an obvious for one skilled in the art to have added a second metal alloy layer as evidenced by Djokic et al. (5,849,170) in the process of Lin (U.S. Patent 6,406,939, hereafter '939) (a) in view of Zuniga-Ortiz et al. (U.S. Patent Application Publication 2003/0080392, hereafter '392) and Bayan et al. (U.S. Patent 6,372,539, hereafter '539) or (b) in view of Applicant's admitted state of the art (pg. 1, lines 5-13) with the expectation of achieving the desired thickness of the metal alloy layer as well as reducing blistering and improving adhesion of the metal alloy layers.

Claims 4-5,7-8,17 and 21: Regarding the composition of the alloy, it has been held that "differences in concentration or temperature will not support the patentability of subject matter

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encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical.” (MPEP 2144.05.II.A.)

Response to Amendment

4. Applicant's arguments filed 3/9/10 have been fully considered but they are not persuasive.

Appellant requested that the Examiner acknowledge the drawings and claim for Foreign priority.

These both have been done in paper filed 11/4/09, however, the Examiner will do so again for Applicant's convenience.

Applicant argued that '939 fails to teach structuring the first metal to the surface of the substrate and that it is the integrated circuit and not the substrate and the seeding is done on the integrated circuit and not the substrate.

The Examiner agrees in part. While the prior art does teach forming the circuitry on the integrated circuit it also teaches forming the circuitry on the dielectric substrate and the via hole formed therein with the use of catalytic sites. The “chip assembly” includes the chip as well as the dielectric substrate with via holes. Hence, the prior art teaches the structuring of the first metal on the substrate and seeding to form the conductive circuit applied thereafter.

Applicant argues that the Examiner has taken Official Notice and has not provided support for this.

The Examiner disagrees. As noted on pg. 3 of the rejection filed 12/9/09, following the Official Notice, the Examiner has provided a citation in the primary reference '939 for support for this position. In fact, this support has been in the rejection since the Final Rejection filed 8/12/05 (see page 3, section 5).

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian K. Talbot whose telephone number is (571) 272-1428. The examiner can normally be reached on Monday-Friday 8AM-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy H. Meeks can be reached on (571) 272-1423. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Brian K Talbot/
Primary Examiner, Art Unit 1715

BKT